

Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-11. (Canceled)

12. (Currently Amended) A method of manufacturing a thin film transistor circuit substrate, comprising the steps of:

forming a plurality of element chips, each having at least one thin film transistor, on a first substrate via a peeling layer;

forming a wiring line on a second substrate;

pressingly attaching at least one element chip of the plurality of element chips in a predetermined position ~~of on~~ on the second substrate via an adhesive, and electrically connecting the at least one element chip and the wiring line; and

peeling the at least one element chip from the first substrate, by irradiating a laser beam onto the peeling layer, after electrically connecting the at least one element chip and the wiring line;

wherein the step of forming the thin film transistor includes the steps of forming an amorphous silicon layer on the peeling layer, crystallizing the amorphous silicon layer by irradiating a laser beam thereonto, and then forming a polycrystalline ~~silicene~~-silicon layer by patterning the crystallized amorphous silicon layer, forming an insulating film on the first substrate and the polycrystalline silicon layer, and forming the gate metal on the insulating film, and then forming a gate electrode by patterning the gate metal; wherein

holographic lithography and a ~~follow~~-dynamic auto focus system are used for patterning the crystallized amorphous silicon layer and the gate metal;

stepper exposure is used for patterning other than patterning the crystallized amorphous silicon layer and the gate metal; and

a design rule finer than a design rule used for the other patterning is used for patterning the crystallized amorphous silicon layer and the gate metal.

13. (Currently Amended) The method according to claim 12, further comprising using the design rule of 1.0 micron or less for the ~~patterning~~patterning of the crystallized amorphous silicon layer and the gate metal.

14. (Previously Presented) The method according to claim 12, the other patterning including the patterning of the crystallized amorphous silicon layer.